Abstract of the Disclosure

A COMPUTER SYSTEM WITH TWO DEBUG WATCH MODES

A computer system is provided with precise and non-precise watch modes. The computer system is a pipelined system in which the fate of an instruction is determined at the decode stage. Once instructions have been decoded, it is not possible for them to be "killed" later in the pipeline. According to the precise watch mode, instructions are held at the decode stage until the guard value has been resolved to determine whether or not that instruction is committed. Actions of the decode unit are determined in dependence on whether or not the instruction is committed when the guard has been resolved. According to a non-precise watch mode, instructions continue to be decoded and executed normally until a breakpoint instruction has had its guard resolved. At that point, an on-chip emulator can take over operations of the processor in a divert mode. The computer system can take into account different intrusion levels while implementing the watch modes.